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(54) Terminal electrode for a chip package, assembly and method of production.

(57) A chip carrier according to the present invention includes: a carrier body including an upper face, a lower face, and an internal conductor; and a plurality of terminal electrodes formed on the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor. A plurality of concave portions for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor are provided on the lower face of the carrier body, the concave portions being electrically connected to the internal conductor.

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BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to: a chip package, a chip carrier, and a method for producing the same; a terminal electrode for a circuit substrate and a method for producing the same; and a complex including the above-mentioned chip package mounted on a circuit substrate (hereinafter, such a complex will be referred to as a "chip package-mounted complex").

2. Description of the Related Art:

In recent years, the integration degrees of LSIs (Large Scale Integrated Circuits) have remarkably improved, and, accordingly, the number of pins included in one LSI chip has been increasing. As for electronic equipment incorporating LSI chip packages, the size and the thickness thereof have been desired to be reduced. Accordingly, a number of high-density mounting techniques for mounting LSI chips on a circuit substrate at a high density have been developed. A variety of shapes and structures have been proposed for such LSI chip packages (NIKKEI ELECTRONICS 1993. 8.2, No. 587, "LSI package frontier, prompting high-density mounting", pp 93 to 99).

In the present specification, the term "chip carrier" refers to a substrate including terminal electrodes (which are to be connected to electrodes of an LSI chip) and contact electrodes (which are to be connected to a circuit substrate). The term "chip package" refers to a chip carrier with an LSI chip mounted thereon. The chip package, as a whole, is to be mounted on a circuit substrate so as to form a "chip package-mounted complex".

Hereinafter, a method for mounting a conventional chip package onto a circuit substrate will be briefly described.

First, a chip carrier is formed in the following manner. Via holes are formed in a printed circuit board by using a laser beam or by a mold punching technique. A ceramic board may be used instead of a printed circuit board. Terminal electrodes are previously formed on both faces of the printed circuit board. Thereafter, an internal conductor in the printed circuit board is electrically connected to the terminal electrodes by a plating technique or the like. Next, an LSI chip is adhered to an upper face of the above-mentioned chip carrier in a face-up state by using a die bond. Thereafter, electrode pads of the LSI chip are connected to the terminal electrodes present on the upper face of the chip carrier by a wire bonding technique. On the resultant composite, a mold res-

in is applied so as to cover the LSI chip and the wire bonding, thereby sealing the composite.

Next, a solder layer is formed on the terminal electrodes provided on a lower face (i.e., the face which opposes the circuit substrate when the chip package is mounted on a circuit substrate) of the printed circuit board by printing or the like. Thereafter, the solder is melted by an infrared reflow technique or the like, so as to form solder balls (having diameters in the vicinity of 700 µm). Thus, a chip carrier is obtained. It is also applicable to adhere previously prepared solder balls onto the terminal electrodes of the chip carrier. Thus, a chip package is obtained.

Furthermore, the chip package is positioned with respect to the circuit substrate in such a manner that the solder balls are located in predetermined positions on the circuit substrate. Then, the chip package is disposed on the circuit substrate. Thereafter, the solder balls are melted by an infrared reflow technique or the like, so as to connect the terminal electrodes on the lower face of the chip package to terminal electrodes of the circuit substrate. Thus, a chip package-mounted complex is obtained.

However, the above-mentioned prior art technique has the following problems:

1. Since wire bonding is conducted for connecting the terminal electrodes of the chip carrier to the electrode pads of the LSI chip, an area occupied by the chip carrier becomes larger than an area occupied by the LSI chip. Moreover, because of the mold resin sealing process conducted after the wire bonding connection, the resultant chip package becomes thicker than the height of the loop height of the wire bonding. This hinders the reduction of the size and the thickness of the chip package.
2. Since signals travel through the wire bonding, which have relatively large lengths, the input/output signals are likely to be delayed. Accordingly, the high-frequency characteristics of the chip package deteriorate, so that the chip package is likely to pick up noises.
3. The solder balls, disposed in an array on the lower face of the chip package, prevent the pitch of the terminals of the LSI chip from being reduced. The solder balls are typically arranged at a pitch as large as about 1 mm.
4. The size of the solder balls determines the distance between the chip package and the circuit substrate. In other words, the interval between the chip package and the circuit substrate cannot be made smaller than the size of the solder balls.
5. In the case where the substrate of the chip carrier is made of a different material from that of the circuit substrate, stresses caused due to a

thermal impact will concentrate on the solder connection portions, thereby creating cracks. As a result, the electrical resistance of the solder connection portions may increase.

SUMMARY OF THE INVENTION

A chip carrier according to the present invention includes: a carrier body including an upper face, a lower face, and an internal conductor; and a plurality of terminal electrodes formed on the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor, wherein a plurality of concave portions for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor are provided on the lower face of the carrier body, the concave portions being electrically connected to the internal conductor.

In one embodiment of the invention, the chip carrier further includes a plurality of contact electrodes electrically connected to the electrodes on the circuit substrate, the contact electrodes being buried in respective ones of the plurality of concave portions, wherein the contact electrodes are composed of a conductive adhesive.

In another embodiment of the invention, the plurality of contact electrodes project from the lower face of the carrier body.

In still another embodiment of the invention, the carrier body includes a plurality of via holes; at least a portion of the internal conductor is composed of a conductive material provided in the plurality of via holes; and at least some of the plurality of concave portions of the carrier body are constituted by the plurality of via holes.

In still another embodiment of the invention, the carrier body is composed of a plurality of insulation sheets layered on one another, the carrier body including a plurality of via holes for connecting the upper face to the lower face, and wherein the internal conductor is composed of a conductive material provided in the plurality of via holes and a conductive layer provided on at least one of the plurality of insulation sheets.

In still another embodiment of the invention, the conductive adhesive has flexibility.

In still another embodiment of the invention, the internal conductor is composed of a material selected from the group consisting of Cu, Ag, and AgPd.

Alternatively, a chip package according to the present invention includes a chip carrier and an LSI chip mounted on the chip carrier in a flip-chip fashion, the chip carrier including: a carrier body including an upper face, a lower face, and an internal conductor; a plurality of terminal electrodes formed on the upper face of the carrier body, the

plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor; and a plurality of concave portions for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor, the concave portions being provided on the lower face of the carrier body, wherein the LSI chip includes: an electrode pad provided on the LSI chip and a projection electrode formed on the electrode pad, the projection electrode being electrically connected to a corresponding one of the terminal electrodes of the chip carrier with a bonding layer interposed therebetween, and an interspace between the LSI chip and the chip carrier being filled with and sealed by a mold resin.

In one embodiment of the invention, the chip package further includes a plurality of contact electrodes electrically connected to the electrodes on the circuit substrate, the contact electrodes being buried in respective ones of the plurality of concave portions, wherein the contact electrodes are composed of a conductive adhesive.

In another embodiment of the invention, the projection electrode of the LSI chip has a two-step convex shape.

In still another embodiment of the invention, the conductive adhesive has flexibility.

In still another embodiment of the invention, the bonding layer is composed of a material selected from the group consisting of a conductive adhesive, an anisotropic conductive material, and solder.

Alternatively, a chip package according to the present invention includes a chip carrier and an LSI chip mounted on the chip carrier in a flip-chip fashion, the chip carrier including: a carrier body including an upper face, a lower face, and an internal conductor; a plurality of terminal electrodes formed on the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor; and a plurality of contact electrodes for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor, the contact electrodes being provided on the lower face of the carrier body, and the contact electrodes being composed of a conductive adhesive and buried in a plurality of concave portions formed on the lower face of the carrier body, wherein the LSI chip includes: an electrode pad provided on the LSI chip and a projection electrode formed on the electrode pad, the projection electrode being electrically connected to a corresponding one of the terminal electrodes of the chip carrier with a bonding layer interposed therebetween, and an interspace between the LSI chip and the chip carrier being filled with and sealed by a mold resin.

In one embodiment of the invention, the projection electrode of the LSI chip has a two-step convex shape.

In another embodiment of the invention, the conductive adhesive has flexibility.

In still another embodiment of the invention, the bonding layer is composed of a material selected from the group consisting of a conductive adhesive, an anisotropic conductive material, and solder.

A method for producing a chip carrier according to the present invention includes the steps of: forming via holes in a plurality of unsintered green sheets; burying a portion of an internal conductor in the via holes of a group of the plurality of green sheets and forming an internal conductor on the group of the plurality of green sheets by printing; obtaining a multilayer structure by layering one of the plurality of solders in which a portion of the internal conductor is not buried in the via holes thereof on the group of green sheets in which the portion of the internal conductor is buried in the via holes and subjecting the multilayer structure to a pressing process; and sintering the plurality of green sheets so as to form a carrier body, a plurality of concave portions being formed on a lower face of the carrier body.

In one embodiment of the invention, the method further includes a step of forming a plurality of contact electrodes by burying a conductive adhesive in the plurality of concave portions of the carrier body.

In another embodiment of the invention, the conductive adhesive has flexibility.

A terminal electrode for a circuit substrate according to the present invention, on which a chip package is mounted, is formed on the circuit substrate and includes: a lower step portion formed on the circuit substrate; and an upper step portion formed on the lower step portion.

In one embodiment of the invention, an area of a cross section of the upper step portion taken on a plane parallel to the circuit substrate is smaller than an area of a cross section of the lower step portion taken on a plane parallel to the circuit substrate.

Alternatively, a method for producing a terminal electrode for a circuit substrate according to the present invention includes the steps of: forming a first resist film on the circuit substrate by a first photolithography process, the first resist film having a first opening on an electrode pad of the circuit substrate; forming a lower step portion of the terminal electrode in the first opening of the first resist film; forming a second resist film on the circuit substrate by a second photolithography process, the second resist film having a second opening on the lower step portion of the terminal electrode and

the second opening being smaller than the first opening of the first resist film; forming an upper step portion of the terminal electrode in the second opening of the second resist film; and removing the first and second resist films, whereby the terminal electrode is formed.

A chip package-mounted complex according to the present invention includes a chip package mounted on a circuit substrate, the chip package including a chip carrier and an LSI chip mounted on the chip carrier in a flip-chip fashion, wherein the chip carrier includes: a carrier body including an upper face, a lower face, and an internal conductor; a plurality of terminal electrodes formed on the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor; and a plurality of contact electrodes for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor, the contact electrodes being provided on the lower face of the carrier body, and the contact electrodes being composed of a conductive adhesive and buried in a plurality of concave portions formed on the lower face of the carrier body, wherein the LSI chip includes: an electrode pad provided on the LSI chip and a projection electrode formed on the electrode pad, the projection electrode being electrically connected to a corresponding one of the terminal electrodes of the chip carrier with a bonding layer interposed therebetween, and an interspace between the LSI chip and the chip carrier being filled with and sealed by a mold resin; and wherein the circuit substrate includes a terminal electrode connected to a corresponding one of the contact electrodes of the chip carrier.

In one embodiment of the invention, the terminal electrode of the circuit substrate projects toward a corresponding one of the concave portions of the carrier body.

In another embodiment of the invention, the terminal electrode of the circuit substrate has a two-step concave shape.

In accordance with the chip carrier according to the present invention, terminal electrodes for mounting an LSI chip in a flip-chip fashion are provided on an upper face of a carrier body. On a lower face of the carrier body, contact electrodes to be connected to electrodes present on a circuit substrate are provided. Moreover, the terminal electrodes and the contact electrodes are electrically interconnected by means of an internal conductor provided within the carrier body. By using such a chip carrier, a circuit on the LSI chip can be connected to a circuit on the circuit substrate without occupying a large space. Since no wire bonding is used for the interconnection between the LSI chip and the circuit substrate, electric signals travel

through a relatively short route created between the LSI chip and the circuit substrate. As a result, the resistor components and capacitor components are reduced, as compared to the case where wire bonding is used, so that the high-frequency characteristics of the chip carrier or the chip package are improved. In addition, by utilizing the internal conductor in the carrier body and the like, it becomes possible to adopt a different arrangement layout for the terminal electrodes from that of the contact electrodes.

Furthermore, the contact electrodes are formed of a conductive adhesive buried in a multitude of concave portions on the lower face of the carrier body. The conductive adhesive serves to, as well as mechanically adhering the carrier body to the circuit substrate, electrically connect the internal conductor of the carrier body to the terminal electrodes of the circuit substrate. By ensuring that the contact electrodes are located in the multitude of concave portions on the lower face of the carrier body, the size of an interspace between the carrier body and the circuit substrate can be reduced. Since the contact electrodes are formed of a conductive adhesive, the interconnection between the contact electrodes and the circuit substrate becomes stable, thereby achieving an improved reliability. In particular, the interconnection becomes resistant against thermal impacts.

In the method for producing a chip carrier according to the present invention, the formation of the contact electrodes is easily achieved by filling the concave portions formed on the lower face of the carrier body with a conductive adhesive.

The chip package according to the present invention, including an LSI chip mounted in a flip-chip fashion on the above-mentioned chip carrier, is compact and thin. Since the step of filling the multitude of concave portions on the lower face of the carrier body can be performed in a relatively simple manner, it is possible for one who has purchased the chip package to conduct the step by himself immediately before mounting the chip package on a circuit substrate.

The terminal electrodes for a circuit substrate, according to the present invention, have a convex shape and therefore are easy to insert into the concave portions constituting the contact electrodes of the chip carrier. In the method for producing the terminal electrodes according to the present invention, minute projection electrodes of a two-step shape can be easily formed with a high yield by adopting a photolithography technique.

In accordance with the chip package-mounted complex of the present invention, contact electrodes are formed of a conductive adhesive, so that a chip carrier can be connected to a circuit substrate in a mechanically/electrically stable manner.

Thus, the invention described herein makes possible the advantages of (1) providing a chip package which has a reduced size and a reduced thickness and excellent high-frequency characteristics and which is capable of being connected to a circuit substrate with a high reliability and stability; (2) providing a chip carrier for the above-mentioned chip package and a method for producing the same; (3) and providing a terminal electrode for a circuit substrate to be suitably used for the above-mentioned chip package and a method for producing the same, and further providing a chip package-mounted complex including the above-mentioned chip package mounted on a circuit substrate.

These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic cross-sectional view showing a chip package according to the present invention.

Figure 2 is a schematic cross-sectional view showing another chip package according to the present invention.

Figure 3 is a schematic cross-sectional view showing a chip carrier according to the present invention.

Figure 4 is a schematic cross-sectional view showing another chip carrier according to the present invention.

Figures 5A to 5I are cross-sectional views for describing the respective steps of a method for producing a chip carrier according to the present invention.

Figure 6 is a cross-sectional view showing convex terminal electrodes for a circuit substrate according to the present invention.

Figures 7A to 7D are cross-sectional views for describing the respective steps of a method for forming the convex terminal electrodes shown in Figure 6.

Figure 8 is a schematic cross-sectional view showing a chip package-mounted complex according to the present invention.

Figure 9 is a schematic cross-sectional view showing another chip package-mounted complex according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the present invention will be described by way of examples, with reference to the

accompanying drawings.

As shown in Figure 1, a chip package 19 according to the present example includes a chip carrier 12 and an LSI chip 7 mounted on the chip carrier 12 in a flip-chip fashion.

The LSI chip 7 includes a plurality of electrode pads 8 and projection electrodes 11 in such a manner that one projection electrode 11 is formed on each electrode pad 8. Any known and suitable LSI chip may be used as the LSI chip 7. The size of the LSI chip 7 to be used in the present invention is typically 10 mm by 10 mm by 0.5 mm. The electrode pads 8 and the projection electrodes 11 are provided in a peripheral portion of the LSI chip 7. The electrode pads 8 and the projection electrodes 11 are used for connecting the wiring of an integrated circuit formed on the LSI chip 7 to an external circuit. The projection electrodes 11 are typically disposed at a pitch in the range of about 0.200 mm to about 0.120 mm at present. Even smaller pitches are likely to be adopted for the projection electrodes 11 in the future. Each projection electrode 11 is electrically connected to one of a plurality of terminal electrodes 6 of the chip carrier 12 with a bonding layer (conductive adhesive) 9 interposed therebetween. The projection electrodes 11 preferably have a two-step convex shape (i.e. a shape consisting of one convex portion lying on top of another), so as to ensure a stable interconnection between the projection electrodes 11 and the terminal electrodes 6 of the chip carrier 12. The bonding layer (conductive adhesive) 9 may be formed of an anisotropic material or solder, instead of a conductive adhesive. An interspace between the LSI chip 7 and the chip carrier 12 is filled with a mold resin 10 so as to be sealed thereby.

Next, the chip carrier 12 will be described in detail, with reference to Figure 3. The chip carrier according to the present example includes a multilayered ceramic substrate as a carrier body 1, the carrier body 1 further including an internal conductor. On an upper face of the carrier body 1, a plurality of terminal electrodes 6 for electrically connecting the projection electrodes 11 of the LSI chip 7 to the internal conductor are provided. On a lower face of the carrier body 1, a plurality of concave portions for electrically connecting electrodes of a circuit substrate (not shown in Figure 3) to the internal conductor are provided. Each concave portion has a depth in the range of about 20 μm to about 100 μm , and an inner diameter of about 200 μm . In each concave portion, one of a plurality of contact electrodes 5 is buried in such a manner that the contact electrodes 5 are in contact with the electrodes on the circuit substrate. In the present example, the contact electrodes 5 project from the lower face of the carrier body 1 by about

10 μm to about 20 μm . However, the contact electrodes 5 do not need to project from the lower face of the carrier body 1 in cases where the electrodes of the circuit substrate have a two-step convex structure, which will be described later.

Each contact electrode 5 is electrically connected to a corresponding one of the terminal electrodes 6 by means of the internal conductor. As a result, an electrical interconnection is achieved between the LSI chip 7 and the circuit substrate (not shown), without using wire bonding. Thus, excellent high-frequency characteristics are provided. In the present example, the internal conductor in the carrier body 1 is composed of vias 3, which are buried in via holes 2 of the carrier body 1, and intra-substrate wiring 4. The internal conductor serves to electrically connect the terminal electrodes 6, which are arranged in a peripheral portion of the upper face of the carrier body 1 at a relatively small pitch, to the contact electrodes 5, which are arranged on the lower face at a relatively large pitch. Since the electrode pads 8 of the LSI chip 7 are disposed in a peripheral portion of the LSI chip 7, the terminal electrodes 6 can only be disposed in the above-mentioned peripheral portion of upper face of the carrier body 1. However, the positions of the contact electrodes 5 are not limited to a peripheral portion of the lower face of the carrier body 1. By utilizing the entire area of the lower face of the carrier body 1 when disposing the contact electrodes 5, it becomes possible to efficiently dispose the contact electrodes 5 at a relatively large pitch. As a result, it becomes easier to prevent adjoining ones of the contact electrodes 5 from being short-circuited. Increasing the pitch of the contact electrodes 5 also allows the size of each contact electrode 5 to be increased. As a result, a highly reliable electrical/mechanical interconnection can be achieved between the contact electrodes 5 and the circuit substrate. In the present example, the minimum allowable pitch of the contact electrodes 5 is about 400 μm . It is also applicable to provide circuit elements, such as resistors and capacitors, in a portion of the intra-substrate wiring 4.

The LSI chip 7 is mounted on the chip carrier 12 in the following manner:

Referring back to Figure 1, the projection electrodes 11, which are composed of Au and have a two-step shape, are formed on the electrode pads 8 of the LSI chip 7 by using a ball bonding method. Thereafter, the conductive adhesive 9 is transcribed onto a tip portion of each projection electrode 11. Next, the projection electrodes 11 are positioned so as to coincide with the terminal electrodes 6 of the chip carrier 12. Thereafter, the LSI chip 7 is disposed on the chip carrier 12, and the conductive adhesive 9 is thermally cured. Then,

the interspace between the LSI chip 7 and the chip carrier 12 is filled with the mold resin 10, and the mold resin 10 is thermally cured. The projection electrodes 11, which are formed on the LSI chip 7, may have any structure, e.g. plated Au bumps, plated solder bumps, or solder ball bumps, as long as they permit flip mounting.

One of the important features of the chip carrier 12 and the chip package 19 according to the present invention is that the contact electrodes 5 of the chip carrier 12 are formed of a conductive adhesive filling the concave portions of the carrier body 1. As the conductive adhesive, a polymeric conductive adhesive manufactured by Ablestik Co., Ltd. (product number #8250) can be used, for example. The contact electrodes 5 being formed of such a conductive adhesive provides the following advantage:

The interspace between the chip package 19 and a circuit substrate on which the chip package 19 is mounted is greatly reduced as compared with the case where electrodes such as solder balls are used. Moreover, such contact electrodes 5 can be easily connected to any of the projection electrodes of the circuit substrate. By inserting the projection electrodes of the circuit substrate into the contact electrodes 5 of the chip package 19, problems such as creeping-up of the adhesive and short-circuiting between the projection electrodes can be prevented relatively easily. Furthermore, a large contact area is secured between the projection electrodes of the circuit substrate and the conductive adhesive, so that a large bonding strength is provided, thereby resulting in an improved reliability. In cases where the conductive adhesive has flexibility, in particular, the contact electrodes 5 become immune to cracks even when receiving a thermal impact.

It is also applicable to use a substrate shown in Figure 4, in which contact electrodes 5 are directly electrically connected to terminal electrodes 6 by means of vias 3, as the carrier body 1 of the chip carrier 12 according to the present invention. An exemplary chip package incorporating such a substrate is shown in Figure 2. In this chip package, no intra-substrate wiring is provided. However, leading wires (not shown) are provided on an upper face of the carrier body 1 so as to extend from the terminal electrodes 6, thereby making it possible to dispose via holes 2 and vias 3 in different positions from where the terminal electrodes 6 are located. Although the designing liberty for the chip carrier shown in Figure 4 is reduced as compared with that for the chip carrier shown in Figure 3, it is still possible to arrange the contact electrodes 5 in a different pattern from that for the terminal electrodes 6 in this manner. Figure 2 shows this chip package in a state where an LSI chip 7 is mounted

on the chip carrier 12.

Next, a method for producing a chip carrier according to the present invention will be described with reference to Figures 5A to 5I.

First, as shown in Figure 5A, via holes 2a and 2b are formed in a plurality of unsintered ceramic green sheets 1a and 1b, respectively, by using a laser beam or by a mold punching method. In the case of forming the carrier body 1 shown in Figure 3, the via holes 2a and 2b have different layout patterns depending on the green sheet 1a or 1b; however, in Figures 5A to 5I, the via holes 2a and 2b are shown to constitute the same layout pattern throughout the green sheets 1a and 1b for conciseness. In the case of forming the carrier body 1 shown in Figure 4, the via holes 2a and 2b have the same layout pattern throughout the green sheets 1a and 1b.

A ceramic green sheet manufactured by Nippon Electric Glass Co., Ltd. (containing MLS-1000 as a main component) may be used as each green sheet 1a or 1b, for example. About five to ten such green sheets, having a thickness of about 200 µm, for example, are layered in order to form one carrier body 1. Such unsintered green sheets 1a and 1b (thickness: 200 µm) will have a thickness of 150 µm after being sintered, so that the carrier body 1 will finally have a thickness in the range of 0.7 mm to 1.5 mm. The thickness of the carrier body 1 is preferably small, so that the thicknesses of the chip carrier and the chip package are reduced.

Next, as shown in Figure 5B, vias 3a are formed by burying a conductive material in the via holes 2a of the green sheets 1a by printing. Thereafter, as shown in Figure 5F, intra-substrate wiring 4a is formed by printing. Thus, the component elements of the internal conductor are formed.

The green sheet 1b, whose via holes 2b have no vias formed therein, is layered on the plurality of green sheets 1a to form a multilayer structure. Thereafter, the multilayer structure is pressed while being heated. Next, as shown in Figure 5G, the layered green sheets 1a and 1b are sintered, whereby the carrier body 1 is formed with a plurality of concave portions 2b provided in a lower face thereof. The concave portions 2b are constituted by the via holes 2b (unfilled) of the lowermost sheet 1b of the carrier body 1. The production steps of the carrier body 1 described heretofore may be replaced by any other conventional method.

After sintering has been conducted, terminal electrodes 6 are formed on an upper face of the carrier body 1, as shown in Figure 5H. Next, as shown in Figure 5I, a conductive adhesive is buried in the plurality of concave portions 2b disposed on a face of the carrier body 1 that opposes a circuit

substrate by being printed through a print mask 14. Squeegees 13 are used for the printing process. Thus, the conductive adhesive is buried in the concave portions 2b of the carrier body 1, so as to form contact electrodes 5. The conductive adhesive may have flexibility. The conductive adhesive includes conductive particles; the conductive particles are preferably formed of AgPd, Au, Ag, Cu or a complex alloy powder.

The contact electrodes 5 filling the concave portions 2b may or may not project from the carrier body 1. In the case where the contact electrodes 5 do not project from the carrier body 1, electrodes provided on the circuit substrate are required to have a shape insertable into the concave portions 2b of the carrier body 1.

In the case where the carrier body 1 is formed by the above-mentioned method, the length of each contact electrode 5, i.e., the size thereof along a direction perpendicular to the lower face of the carrier body 1, is determined in accordance with the thickness of the green sheet 1b constituting the lowermost layer of the carrier body 1. If the green sheet 1b has a thickness of 150 μm after the sintering, each contact electrode 5 has a length in the range of 150 μm to 170 μm . If the length of each contact electrode 5 is increased, the relatively large electrical resistance component which the contact electrodes 5 have becomes unnegligible. Therefore, the length of the contact electrodes 5 is preferably maintained equal to or smaller than about 200 μm .

In cases where the internal conductor is a base metal, inner side faces of the via holes 2b may be plated with a non-oxidizable conductor such as Au before filling the conductive adhesive in the via holes 2b of the green sheet 1b. By conducting such a plating, the area in which the conductive adhesive electrically contacts the internal conductor increases, so that the electrical resistance between the contact electrodes 5 and the internal conductor can be reduced.

The step of forming the contact electrodes 5 may be performed either before or after mounting the LSI chip 7 on the terminal electrodes 6 of the carrier body 1. In some cases, a chip package which includes the LSI chip 7 mounted on the chip carrier but does not include the contact electrodes 5 may be sold to a user. In such cases, the contact electrodes 5 will be buried in the concave portions 2b on the lower face of the carrier body 1 at least before the chip package is mounted on a circuit substrate.

The material of the carrier body 1 may be alumina having good radiation properties, instead of a glass ceramic.

In the case where the chip carrier shown in Figure 4 is produced, the formation of the intra-

substrate wiring 4 is omitted, so that the steps shown in Figures 5A to 5E are performed. Figures 5C to 5E correspond to Figures 5G to 5I, respectively.

Next, the structure of electrodes of a circuit substrate 17 suitable for the chip carrier 12 and the chip package 19 will be described with reference to Figure 6. The circuit substrate 17 includes terminal electrodes 6 of a two-step convex shape. These terminal electrodes 6 are suitably used in the case where the contact electrodes 5 of the carrier body 1 do not substantially project from the lower face of the carrier body 1.

The circuit substrate 17 shown in Figure 6 includes electrode pads 16 formed on an upper face thereof. The circuit substrate 17 further includes the terminal electrodes 18 on the electrode pads 16, each terminal electrode 18 having a two-step convex shape. Each terminal electrode 18 has a lower step portion formed on the circuit substrate 17 and an upper step portion formed on the lower step portion. The shape of the terminal electrodes 18 may be either circular or rectangular when seen from above the circuit substrate 17. The area of a cross section of the upper step portion, taken in parallel to the circuit substrate 17, is preferably smaller than the area of the lower step portion taken on the same plane. The terminal electrodes 18 can be formed of platable metals such as Au, Cu, Ag, and solder. The electrode pads 16 may be formed of any platable material. The circuit substrate 17 may include via holes 22, vias 23, and intra-substrate wiring 24 as shown in Figure 6.

Next, a method for forming the two-step convex terminal electrodes 18 on a circuit substrate will be described with reference to Figures 7A to 7D.

First, as shown in Figure 7A, a resist film A is formed on the circuit substrate 17, on which the electrode pads 16 are provided, by a photolithography process. The resist film A has openings (inner diameter: about 250 μm) formed on those electrode pads 16 which are to be connected to the contact electrodes 5 of the chip carrier 12.

Next, as shown in Figure 7B, the lower step portions 18a (thickness: about several dozen μm) of the terminal electrodes 18 are deposited in the openings of the resist film A. Thus, the lower step portions 18a of the terminal electrodes 18 are selectively formed in the regions of the circuit substrate 17 which are not covered by the resist film A. The shape and size of the lower step portions 18a of the terminal electrodes 18 are determined by the shape and size of the openings of the resist film A. The layout pattern for the lower step portions 18a is determined by that of the openings of the resist film A.

Then, as shown in Figure 7C, a resist film **B** is formed on the circuit substrate 17 by a photolithography process. The resist film **B** has an opening (inner diameter: about 100 μm) in the vicinity of the center of the lower step portion 18a of each terminal electrode 18. The openings of the resist film **B** are formed so as to be smaller than the openings of the resist film **A**. Next, as shown in Figure 7D, the upper step portions 18b (height: about several dozen μm) of the terminal electrodes 18 are deposited by plating.

Finally, the resist films **A** and **B** are removed by being dissolved or peeled. Thereafter, if necessary, a cleaning process is performed, so as to obtain the terminal electrodes 18 having a two-step convex shape on the electrode pads 16 of the circuit substrate 17.

The present invention does not provide any particular limitations to the plating material. Any platable metal, such as Au, Cu, Ag, and solder, can be used as the plating material.

Next, a process for mounting the chip package according to the present invention on the above-mentioned circuit substrate will be described with reference to Figure 8.

After forming the contact electrodes 5 of the chip package 19 with the use of a conductive adhesive, the contact electrodes 5 are positioned so that the position of each contact electrode 5 coincides with the position of the corresponding one of the terminal electrodes 18 of the circuit substrate 17. The circuit substrate 17 used herein includes via holes and intrasubstrate wiring.

Thereafter, the terminal electrodes 18 are inserted into the concave portions of the chip package 19. The contact electrodes 5 are previously filled in the concave portions of the chip package 19. Then, the conductive adhesive constituting the contact electrodes 5 is cured at 50°C to 150°C. Thus, the contact electrodes 5 are electrically/mechanically connected to the terminal electrodes 18, whereby the chip package 19 is mounted on the circuit substrate 17. A chip package-mounted complex thus obtained has the following advantages: A firm connection is achieved between the contact electrodes 5 and the terminal electrodes 18 of the circuit substrate 17. Even if the thermal expansion coefficient of the circuit substrate 17 is different from that of the carrier body 1, the carrier body 1 is not likely to have cracks. In cases where the conductive adhesive has flexibility, in particular, the contact electrodes 5 can have excellent reliability against thermal impacts. In addition, the distance, (i.e. the interspace) between the carrier body 1 and the circuit substrate 17 is reduced, so that the entire thickness of the chip package-mounted complex can be reduced.

Figure 9 shows a chip package-mounted complex including the chip package 19 mounted on a circuit substrate 17 that includes no projection electrodes 18. In this example, the contact electrodes 5 are directly adhered to the electrode pads 16 of the circuit substrate 17.

As described above, according to the examples of the present invention, the LSI chip 7 is mounted on the chip carrier 12 in a flip-chip fashion, so that the chip package 19 occupies a relatively small area and is thin. In addition, the wiring within the chip package 19 extends for a relatively small distance, thereby achieving excellent frequency characteristics.

Furthermore, the contact electrodes 5 of the chip carrier 12 are formed of a conductive adhesive buried in the concave portions on the lower face of the carrier body 1. By inserting the two-step convex shape terminal electrodes 18 formed on the electrode pads 16 of the circuit substrate 17 into the contact electrodes 5, stable interconnection can be achieved between the terminal electrodes 18 and the contact electrodes 5. The entire thickness of a chip package-mounted complex, obtained by mounting the chip package 19 on the circuit substrate 17, can also be reduced.

Thus, according to the present invention, a chip package (including an LSI chip mounted on a chip carrier) is provided which occupies a relatively small area. Moreover, after the chip package is mounted on a circuit substrate, the thickness of the chip package as measured from the circuit substrate is kept small. Therefore, the chip package according to the present invention is ideal for high-density mounting.

Since contact electrodes of the chip package are formed of a conductive adhesive which preferably has flexibility, the chip package can be mounted on a circuit substrate by inserting two-step projection electrodes formed on terminal electrodes of the circuit substrate into the contact electrodes while maintaining the thickness of the resultant circuit module obtained after the mounting.

Furthermore, when the two-step convex terminal electrodes formed on the circuit substrate are inserted into the contact electrodes of the chip package, the convex shape of the terminal electrodes prevents creeping-up of the adhesive and short-circuiting between adjoining terminal electrodes. Moreover, such terminal electrodes come in contact with the conductive adhesive with a high probability and in a large adhesion area. As a result, large adhesion strength can be provided, thereby increasing the reliability of the bonding.

Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the

scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be broadly construed.

Claims

1. A chip carrier comprising:
a carrier body comprising an upper face, a lower face, and an internal conductor; and
a plurality of terminal electrodes formed on the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor,
wherein a plurality of concave portions for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor are provided on the lower face of the carrier body, the concave portions being electrically connected to the internal conductor. 5
2. A chip carrier according to claim 1 further comprising a plurality of contact electrodes electrically connected to the electrodes on the circuit substrate, the contact electrodes being buried in respective ones of the plurality of concave portions, wherein the contact electrodes are composed of a conductive adhesive. 10
3. A chip carrier according to claim 1, wherein the plurality of contact electrodes project from the lower face of the carrier body. 15
4. A chip carrier according to claim 1, wherein:
the carrier body includes a plurality of via holes;
at least a portion of the internal conductor is composed of a conductive material provided in the plurality of via holes; and
at least some of the plurality of concave portions of the carrier body are constituted by the plurality of via holes. 20
5. A chip carrier according to claim 1, wherein the carrier body is composed of a plurality of insulation sheets layered on one another, the carrier body including a plurality of via holes for connecting the upper face to the lower face, and wherein the internal conductor is composed of a conductive material provided in the plurality of via holes and a conductive layer provided on at least one of the plurality of insulation sheets. 25
6. A chip carrier according to claim 2, wherein the conductive adhesive has flexibility. 30
7. A chip carrier according to claim 1, wherein the internal conductor is composed of a material selected from the group consisting of Cu, Ag, and AgPd. 35
8. A chip package comprising a chip carrier and an LSI chip mounted on the chip carrier in a flip-chip fashion, the chip carrier comprising:
a carrier body comprising an upper face, a lower face, and an internal conductor;
a plurality of terminal electrodes formed on the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor; and
a plurality of concave portions for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor, the concave portions being provided on the lower face of the carrier body, 40
9. A chip package according to claim 8 further comprising a plurality of contact electrodes electrically connected to the electrodes on the circuit substrate, the contact electrodes being buried in respective ones of the plurality of concave portions, wherein the contact electrodes are composed of a conductive adhesive. 45
10. A chip package according to claim 8, wherein the projection electrode of the LSI chip has a two-step convex shape. 50
11. A chip package according to claim 8, wherein the conductive adhesive has flexibility. 55
12. A chip package according to claim 8, wherein the bonding layer is composed of a material selected from the group consisting of a conductive adhesive, an anisotropic conductive material, and solder. 60
13. A chip package comprising a chip carrier and an LSI chip mounted on the chip carrier in a flip-chip fashion, the chip carrier comprising:
a carrier body comprising an upper face, a lower face, and an internal conductor;
a plurality of terminal electrodes formed on 65

- the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor; and
- a plurality of contact electrodes for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor, the contact electrodes being provided on the lower face of the carrier body, and the contact electrodes being composed of a conductive adhesive and buried in a plurality of concave portions formed on the lower face of the carrier body,
- wherein the LSI chip comprises:
- an electrode pad provided on the LSI chip and a projection electrode formed on the electrode pad, the projection electrode being electrically connected to a corresponding one of the terminal electrodes of the chip carrier with a bonding layer interposed therebetween, and an interspace between the LSI chip and the chip carrier being filled with and sealed by a mold resin.
14. A chip package according to claim 13, wherein the projection electrode of the LSI chip has a two-step convex shape.
15. A chip package according to claim 13, wherein the conductive adhesive has flexibility.
16. A chip package according to claim 13, wherein the bonding layer is composed of a material selected from the group consisting of a conductive adhesive, an anisotropic conductive material, and solder.
17. A method for producing a chip carrier comprising the steps of:
- forming via holes in a plurality of unsintered green sheets;
- burying a portion of an internal conductor in the via holes of a group of the plurality of green sheets and forming an internal conductor on the group of the plurality of green sheets by printing;
- obtaining a multilayer structure by layering one of the plurality of solders in which a portion of the internal conductor is not buried in the via holes thereof on the group of green sheets in which the portion of the internal conductor is buried in the via holes and subjecting the multilayer structure to a pressing process; and
- sintering the plurality of green sheets so as to form a carrier body, a plurality of concave portions being formed on a lower face of the carrier body.
- 5 18. A method for producing a chip carrier according to claim 17 further comprising a step of forming a plurality of contact electrodes by burying a conductive adhesive in the plurality of concave portions of the carrier body.
- 10 19. A method for producing a chip carrier according to claim 18, wherein the conductive adhesive has flexibility.
- 15 20. A terminal electrode for a circuit substrate on which a chip package is mounted, wherein the terminal electrode is formed on the circuit substrate and comprises:
- a lower step portion formed on the circuit substrate; and
- an upper step portion formed on the lower step portion.
- 20 21. A terminal electrode for a circuit substrate according to claim 20, wherein an area of a cross section of the upper step portion taken on a plane parallel to the circuit substrate is smaller than an area of a cross section of the lower step portion taken on a plane parallel to the circuit substrate.
- 25 22. A method for producing a terminal electrode for a circuit substrate, the method comprising the steps of:
- forming a first resist film on the circuit substrate by a first photolithography process, the first resist film having a first opening on an electrode pad of the circuit substrate;
- forming a lower step portion of the terminal electrode in the first opening of the first resist film;
- forming a second resist film on the circuit substrate by a second photolithography process, the second resist film having a second opening on the lower step portion of the terminal electrode and the second opening being smaller than the first opening of the first resist film;
- forming an upper step portion of the terminal electrode in the second opening of the second resist film; and
- removing the first and second resist films, whereby the terminal electrode is formed.
- 30 23. A chip package-mounted complex comprising a chip package mounted on a circuit substrate, the chip package comprising a chip carrier and an LSI chip mounted on the chip carrier in a flip-chip fashion, wherein the chip carrier comprises:
- a carrier body comprising an upper face, a lower face, and an internal conductor;
- 35 30
- 40 35
- 45 40
- 50 45
- 55 50

a plurality of terminal electrodes formed on the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor; and

a plurality of contact electrodes for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor, the contact electrodes being provided on the lower face of the carrier body, and the contact electrodes being composed of a conductive adhesive and buried in a plurality of concave portions formed on the lower face of the carrier body,

wherein the LSI chip comprises:

an electrode pad provided on the LSI chip and a projection electrode formed on the electrode pad, the projection electrode being electrically connected to a corresponding one of the terminal electrodes of the chip carrier with a bonding layer interposed therebetween, and an interspace between the LSI chip and the chip carrier being filled with and sealed by a mold resin, and

wherein the circuit substrate comprises a terminal electrode connected to a corresponding one of the contact electrodes of the chip carrier.

24. A chip package-mounted complex according to claim 23, wherein the terminal electrode of the circuit substrate projects toward a corresponding one of the concave portions of the carrier body.

25. A chip package-mounted complex according to claim 24, wherein the terminal electrode of the circuit substrate has a two-step concave shape.

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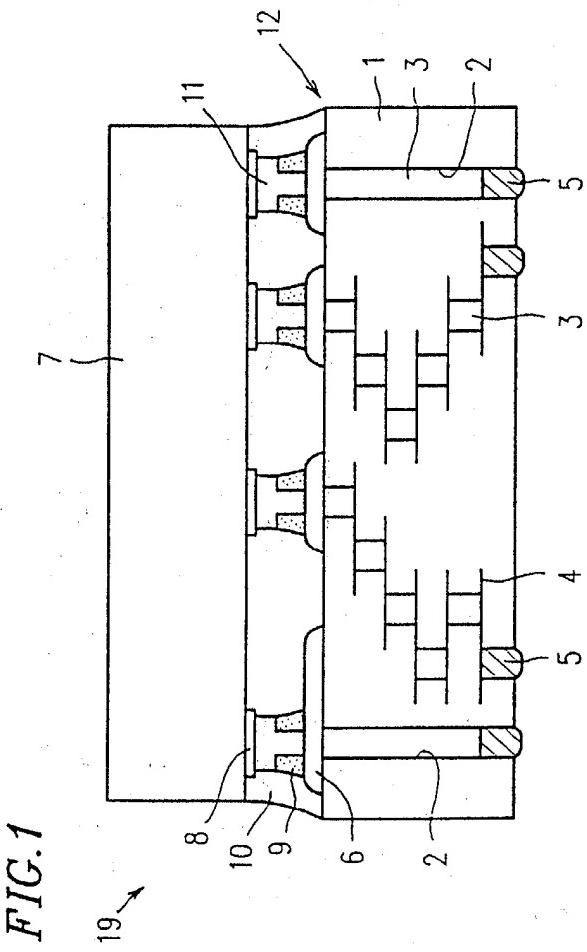
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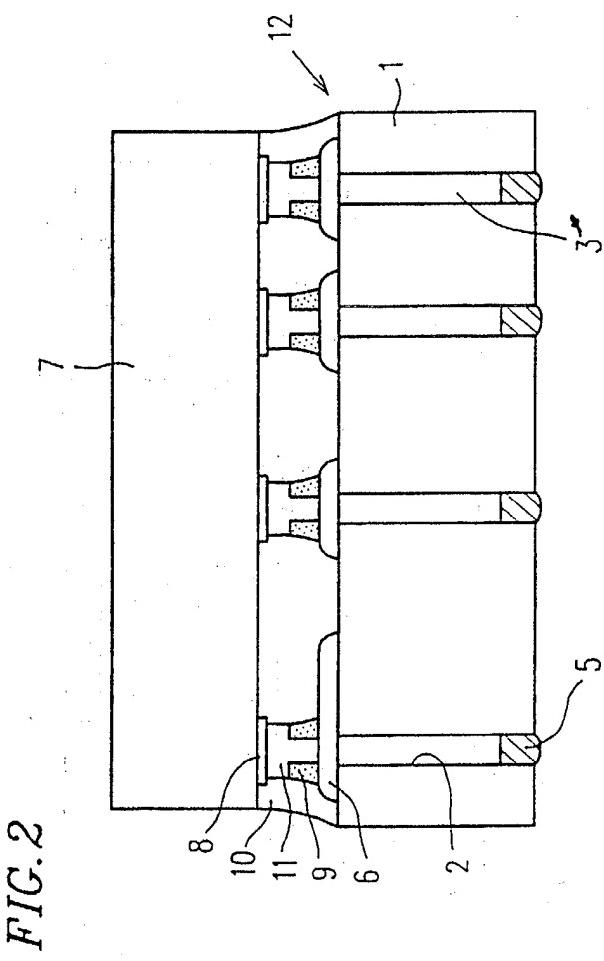
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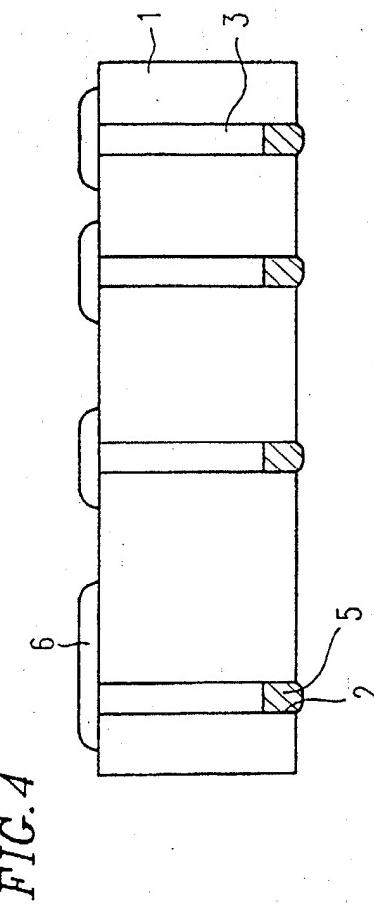
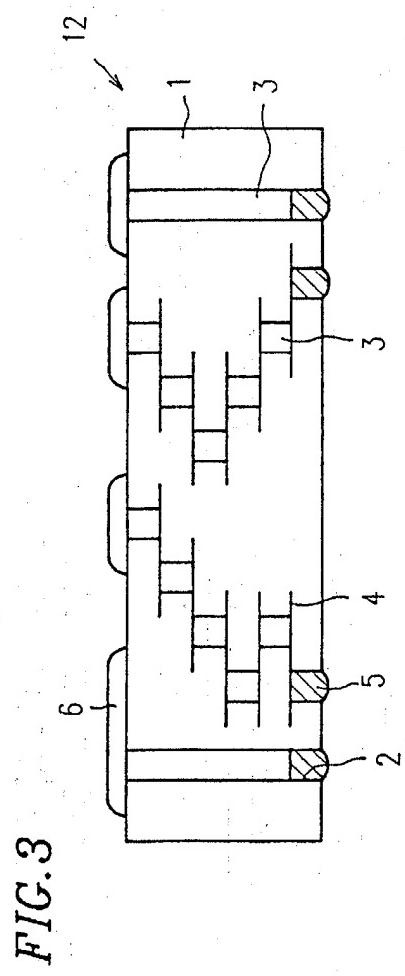
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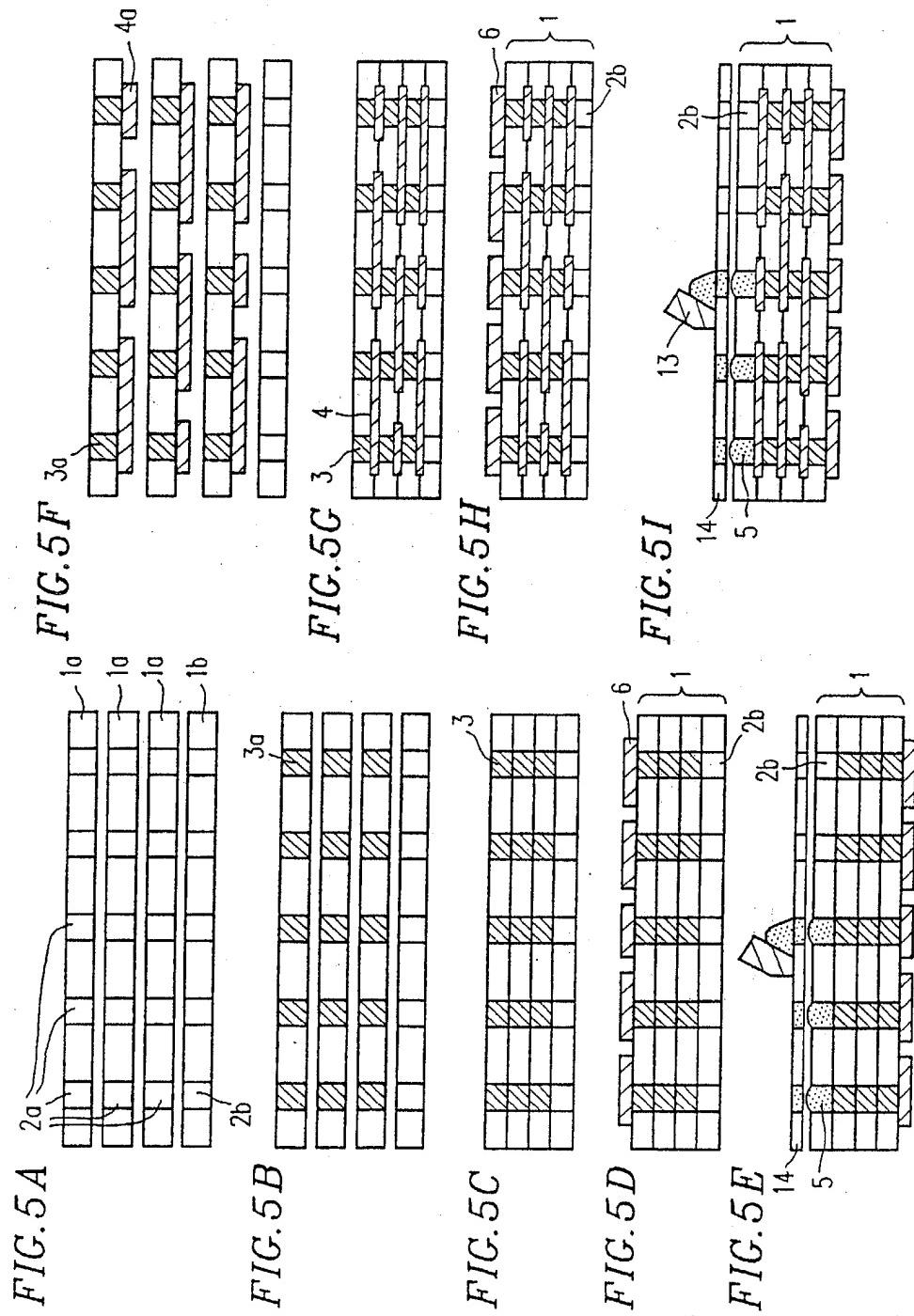
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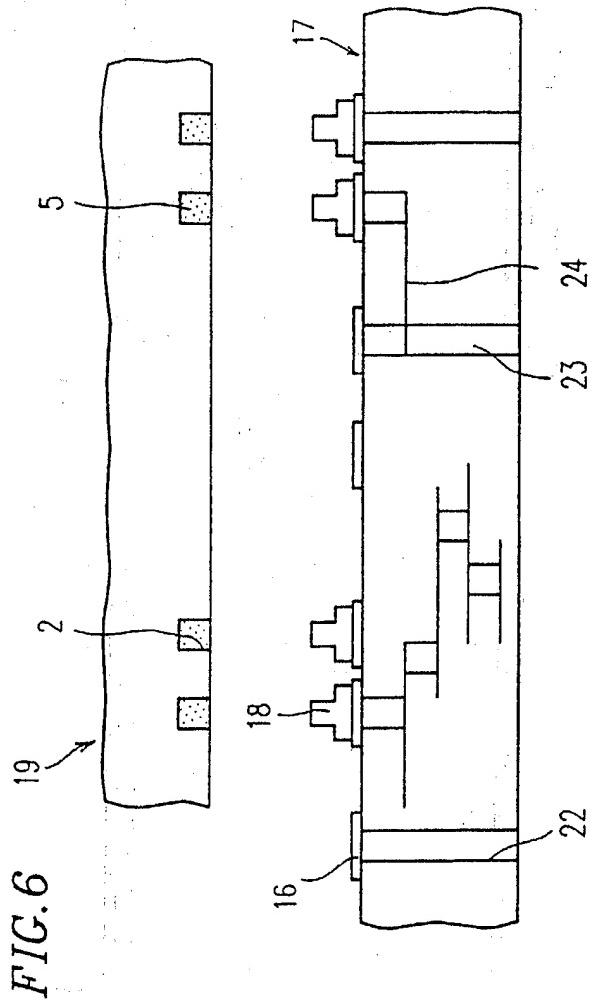
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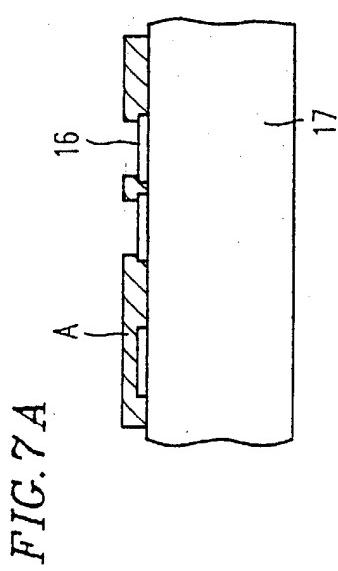


FIG. 7C

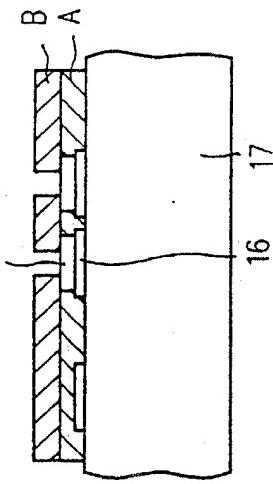


FIG. 7B

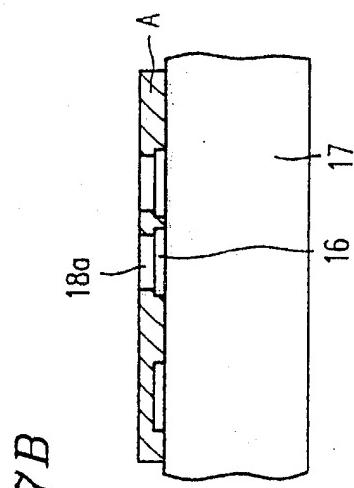
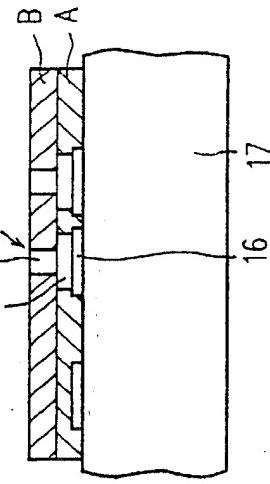
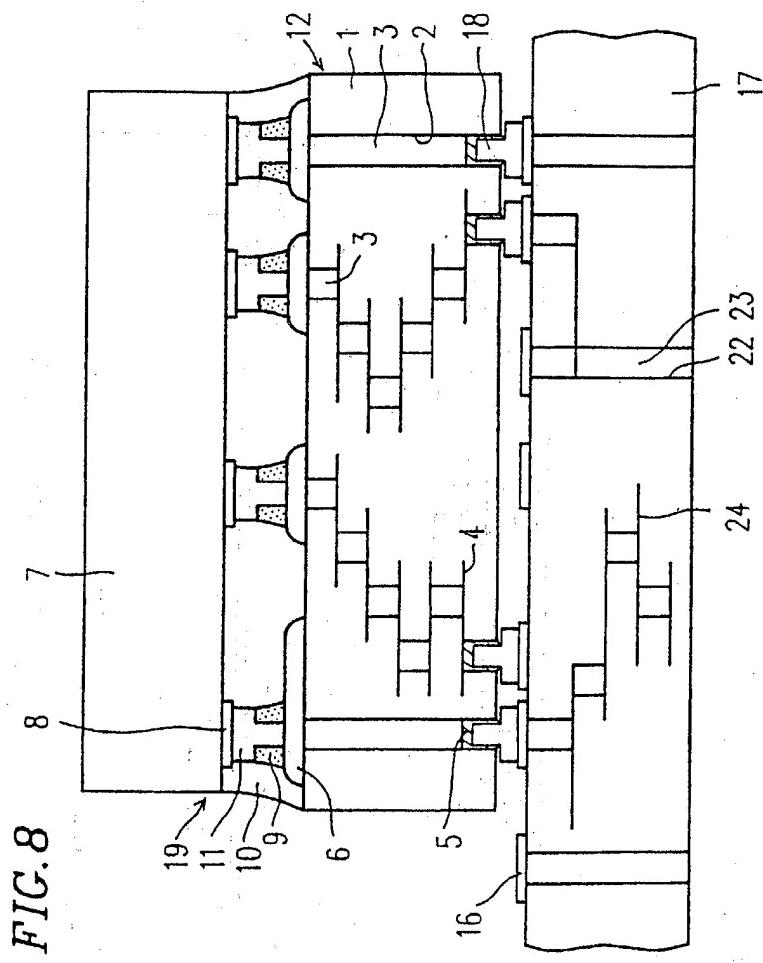
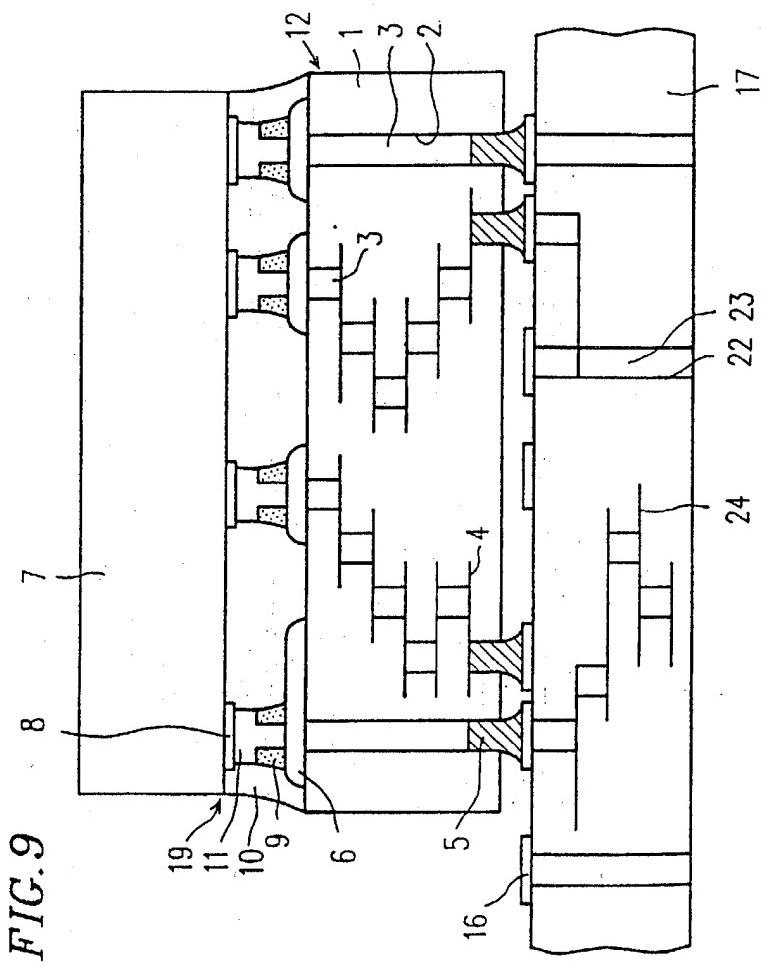
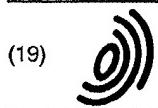


FIG. 7D









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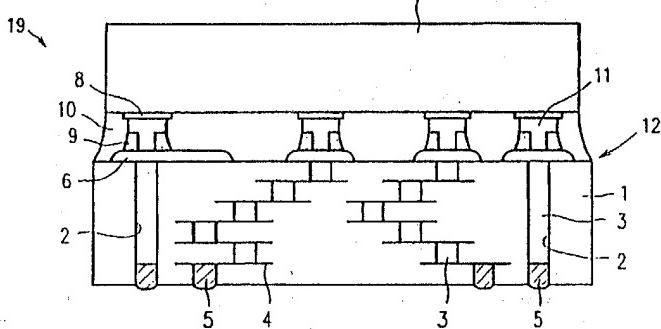
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(54) Terminal electrode for a chip package, assembly and method of production

(57) A chip carrier according to the present invention includes: a carrier body including an upper face, a lower face, and an internal conductor; and a plurality of terminal electrodes formed on the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor. A plurality

of concave portions for electrically connecting a plurality of electrodes on a circuit substrate to the internal conductor are provided on the lower face of the carrier body, the concave portions being electrically connected to the internal conductor.

FIG. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 94 11 9486

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	US-A-5 213 676 (REELE ET AL.) * abstract; figure 4 *	20,21	H01L23/498 H01L21/48
X	EP-A-0 265 631 (IBM) * the whole document *	20,21	
Y	US-A-5 196 089 (TAKADA ET AL.) * the whole document *	22	
Y	EP-A-0 514 723 (HITACHI) * figure 16A-16B *	22	
Y	US-A-5 260 518 (Y. TANAKA ET AL.) * column 5, line 41 - line 55; figures *	1-6,8,9, 11-13, 15-19, 23,24	
Y	ONDE ELECTRIQUE, vol. 73, no. 6; November 1993 PARIS FR, pages 48-54, G. NICOLAS ET AL. 'Evolution des technologies d'interconnexion et d'encapsulation des composants électroniques' * figure 4 *	1-6,8,9, 11-13, 15-19, 23,24	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
Y	PATENT ABSTRACTS OF JAPAN vol. 10 no. 175 (E-413) ,20 June 1986 & JP-A-61 024253 (HITACHI SEISAKUSHO KK) * abstract *	1-6,8,9, 11-13, 15-19, 23,24	H01L
A	EP-A-0 520 434 (HUGHES AIRCRAFT) * figures *	1-25	
		-/-	
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	15 December 1995	Prohaska, G	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
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EUROPEAN SEARCH REPORT

Application Number
EP 94 11 9486

DOCUMENTS CONSIDERED TO BE RELEVANT									
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)						
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A	US-A-5 316 788 (DIBBLE ERIC P ET AL) 31 May 1994 * the whole document * & JP-A-05 206 209 (...) 13 August 1993	1-19, 23-25							
A	US-A-5 118 386 (KATAOKA ET AL.) * the whole document *	22							
A	EP-A-0 536 418 (CITIZEN WATCH CO LTD) 14 April 1993		TECHNICAL FIELDS SEARCHED (Int.Cl.6)						
A	PATENT ABSTRACTS OF JAPAN vol. 9 no. 8 (E-289) , 12 January 1985 & JP-A-59 158539 (SHARP KK)								
A	PATENT ABSTRACTS OF JAPAN vol. 7 no. 84 (E-169) , 7 April 1983 & JP-A-58 010841 (MITSUBISHI DENKI KK)								
P,A	US-A-5 315 239 (VITRIOL WILLIAM A) 24 May 1994 * abstract; figures *	1-19, 23-25							
<p>The present search report has been drawn up for all claims</p> <table border="1"> <tr> <td>Place of search</td> <td>Date of completion of the search</td> <td>Examiner</td> </tr> <tr> <td>THE HAGUE</td> <td>15 December 1995</td> <td>Prohaska, G</td> </tr> </table>				Place of search	Date of completion of the search	Examiner	THE HAGUE	15 December 1995	Prohaska, G
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THE HAGUE	15 December 1995	Prohaska, G							
CATEGORY OF CITED DOCUMENTS									
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application I : document cited for other reasons & : member of the same patent family, corresponding document							
EPO FORM 1593 03.82 (P04C01)									



EP 94 119486.2

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.
namely claims:
- No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions.
namely:

- All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.
namely claims:
- None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.
namely claims:

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EP 94119486.2 - B -

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-19, 23-25: Chip carrier with concave electrode portions.
2. Claims 20-22: Terminal electrode for printed circuit board which projects upward in two steps. --